DATA SHEET

PCD3360
Programmable multi-tone telephone ringer

Product specification
Supersedes data of August 1985
File under Integrated Circuits, IC03

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Philips
Semiconductors

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CONTENTS

1 FEATURES

- Output signals for electro-dynamic transducer (loudspeaker) or for piezo-electric transducer (PXE)
- 7 basic output frequencies (tones) and a pause
- 4 selectable tone sequences
- 4 selectable repetition rates
- 3 selectable impedance settings
- 3-step automatic swell
- Delta-modulated output signal that approximates a sinewave
- Input ringing frequency discriminator with selectable upper and lower frequency limits
- Output for optical signal
- Customized tone sequences, impedance settings and automatic swell levels are mask programmable.

2 GENERAL DESCRIPTION

The PCD3360 is a CMOS integrated circuit, designed to replace the electro-mechanical bell in telephone sets. It meets most postal requirements, with selectivity of output tone sequences and input ringer frequencies. Output signals for a loudspeaker or for a piezo-electric (PXE) transducer are provided. No audio transformer is required since the loudspeaker is driven in class D.

3 QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
f_{TONE}	available frequencies (tones)		553, 600, 667, 800, 1000, 1067, 1333	Hz
n_{int}	number of intervals per tone sequence		15 or 16	
f_{LL}	lower limits of frequency discriminator		13.33 or 20	Hz
f_{UL}	upper limits of frequency discriminator		30 or 60	Hz
Z_{set}	impedance settings	with 50 Ω loudspeaker	≈7, ≈10.5 or ≈17.5	kΩ
$t_{d(on)}$	switch-on delay	ringer frequency = 25 Hz	60 (maximum)	ms

4 ORDERING INFORMATION

TYPE NUMBER	PACKAGE		
	NAME	DESCRIPTION	VERSION
PCD3360P	DIP16	plastic dual in-line package; 16 leads (300 mil)	SOT38-4
PCD3360T	SO16	plastic small outline package; 16 leads; body width 7.5 mm	SOT162-1

5 BLOCK DIAGRAM

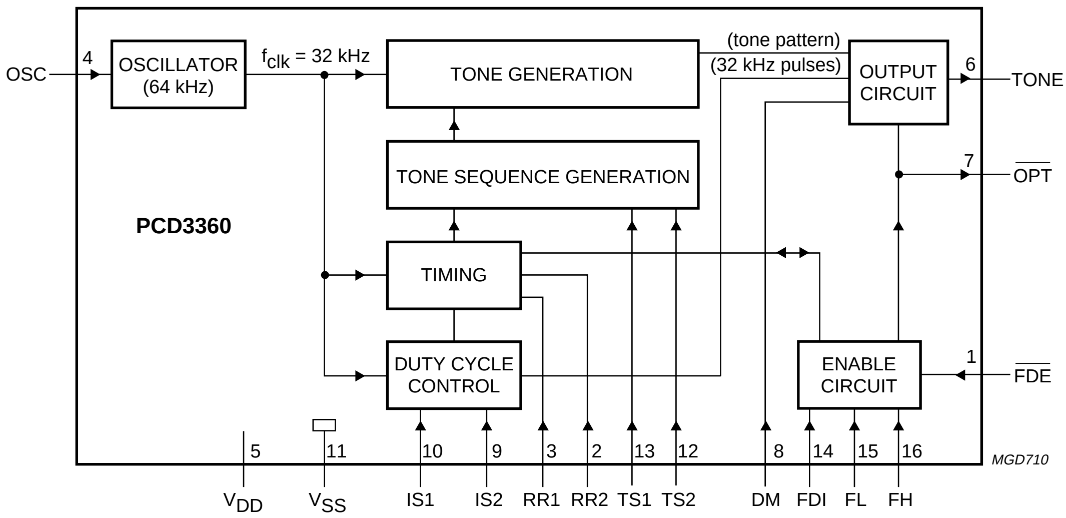


Fig.1 Block diagram.

6 PINNING INFORMATION

6.1 Pinning

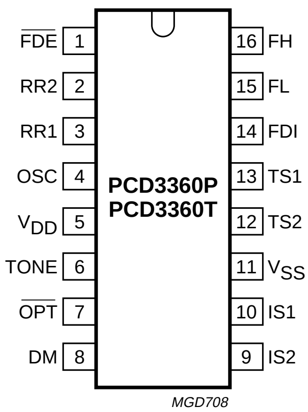


Fig.2 Pin configuration.

6.2 Pin description

Table 1 Pin description, PCD3360

SYMBOL	PIN	TYPE	DESCRIPTION
$\overline{FDE}$	1	I	frequency discriminator enable
RR2, RR1	2, 3	I	repetition rate selection
OSC	4	I	oscillator
V_{DD}	5	P	positive supply
TONE	6	O	tone output
$\overline{OPT}$	7	O	optical signal output
DM	8	I	drive mode selection
IS2, IS1	9, 10	I	impedance setting and automatic swell
V_{SS}	11	P	ground
TS2, TS1	12, 13	I	tone sequence selection
FDI	14	I	frequency discriminator input
FL, FH	15, 16	I	lower and upper frequency limit selection

7 FUNCTIONAL DESCRIPTION (see Fig.1)

7.1 Supply pins (V_{DD} and V_{SS})

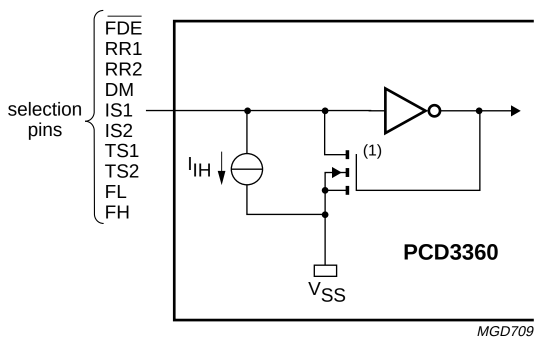
If the supply current (V_{DD}) drops below the standby voltage (V_{stb}), the oscillator and most other functions are switched off and the supply current is reduced to the standby current (I_{stb}). The automatic swell register retains its information until V_{DD} drops further to a value V_{AS} at which reset occurs.

7.2 Oscillator (OSC)

The 64 kHz oscillator is operated via an external resistor and capacitor connected to pin OSC (see Fig.8).
The oscillator signal is divided by two to provide the 32 kHz internal system clock.

7.3 Selection pin input circuit (see Fig.3)

Pins FDE, RR1, RR2, DM, IS1, IS2, TS1, TS2, FL and FH are pulled down internally by a pull-down current I_{IH} when they are connected to V_{DD} and by a pull-down resistance R_{IL} when they are connected to V_{SS}. Thus when the pins are open-circuit they are defined LOW. Therefore only a single-contact switch is required to connect the pins to V_{DD}; yet the supply current is only marginally increased as I_{IH} is very small.



(1) Transistor resistance is R_{IL} when switched on.

Fig.3 Input circuit of selection pins.

7.4 Frequency discriminator circuit ($\overline{\text{FDE}}$ and FDI)

The frequency discriminator circuit prevents the ringer being activated unintentionally by dial pulses, speech or other invalid signals.

The circuit is enabled or disabled by input FDE. When $\overline{\text{FDE}}$ is LOW and $V_{DD} > V_{stb}$, the circuit is enabled and FDI acts as the input for ringing frequency detection. When FDE is HIGH, the circuit is disabled and FDI becomes the enable/disable input for tone sequence generation.

When the circuit is enabled, it starts to produce output ringing tones after one cycle of an appropriate input frequency is detected at FDI. An input cycle is detected when either 2 rising or 2 falling edges are received, and this implies a delay of between 1 and 1.5 input cycles before output ringing begins. The allowed input frequency range is set by the states of pins FL and FH, as shown in Table 2. Output ringing continues for as long as valid input ringing frequency is detected.

FDI has a Schmitt-trigger action; the levels are set by an external resistor R2 (see Fig.8) and an internal sink current that is switched from 20 µA (typ.) for FDI = LOW to <0.1 µA for FDI = HIGH. Excess current entering FDI via R2 is absorbed by internal diodes clamped to V_{DD} and V_{SS}.

7.5 Selection of frequency discriminator limits (FL and FH)

With the frequency discriminator enabled ($V_{DD} > V_{stb}$ and $\overline{\text{FDE}}$ = LOW) the lower and upper limits of the input frequency are set by the inputs FL and FH as shown by Table 2.

Table 2 Selection of lower and upper frequency discriminator limits (f_{OSC} = 64 kHz)

FL INPUT STATE	LOWER LIMIT	FH INPUT STATE	UPPER LIMIT
LOW	20 Hz	LOW	60 Hz
HIGH	13.3 Hz	HIGH	30 Hz

7.6 Selection of tone sequences (TS1 and TS2)

TS1 and TS2 are effective when both $\overline{FDE}$ and FDI are HIGH, and $V_{DD} > V_{stb}$. TS1 and TS2 normally select one of the four standard tone sequences shown in Fig.4. Different tone sequences of 15 or 16 consecutive tones and pauses can be mask programmed to order. The seven tones (plus pause) available are shown in Fig.5, together with the corresponding ROM codes.

The tone sequences are repeated continuously provided the enable conditions at inputs FDE and FDI are valid and $V_{DD} > V_{stb}$. The first sequence and subsequent repetitions always begin with the first note in the sequence.

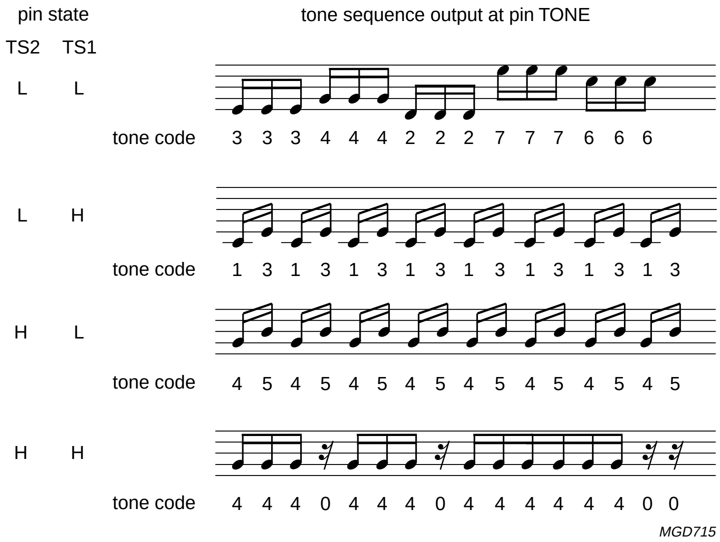


Fig.4 Tone sequences mask-programmed in the PCD3360.

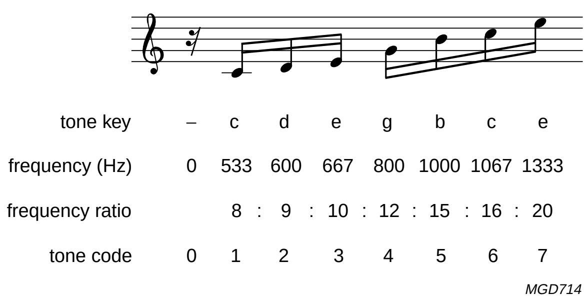


Fig.5 Available tones (including pause) and their corresponding ROM codes.

7.7 Selection of repetition rates (RR1 and RR2)

The duration of a time interval within a tone sequence is determined by the state of inputs RR1 and RR2 as shown in Table 3. The resultant variation of repetition rates acts as a distinguishing feature between adjacent telephones.

Table 3 Duration of time intervals (f_{OSC} = 64 kHz)

INPUT STATE		TIME INTERVAL (ms)
RR1	**RR2**	
LOW	LOW	15
LOW	HIGH	30
HIGH	LOW	45
HIGH	HIGH	60

The repetition rate variation can be extended by mask programming the same tone combination for all 4 tone sequences, but with a different number of time intervals per tone. Thus the repetition rate can be selected from 16 values by inputs RR1, RR2, TSI and TS2. The single tone sequence used is customer-defined.

7.8 Drive mode selection (DM)

The output signal at pin TONE can be selected for application with electro-dynamic or piezo-electric transducers. An example of both signals, for a tone frequency of 667 Hz, is shown in Fig.6.

7.8.1 LOUDSPEAKER MODE

In the loudspeaker mode (DM = LOW), pin TONE outputs a delta-modulated signal that approximates a sinewave sampled at a rate of 32 kHz. The output pulse duration is determined by pins IS1 and IS2. The resultant acoustic spectrum is aurally more acceptable and has greater penetration than a square-wave spectrum because more power is concentrated at the fundamental frequency.

7.8.2 PXE MODE

In the PXE mode (DM = HIGH), pin TONE outputs a square wave. In this mode the ringer impedance and sound pressure level are determined by characteristics (e.g. the size) of the PXE transducer; inputs IS1 and IS2 are inactive.

7.9 Setting of impedance, sound pressure level and automatic swell (IS1 and IS2)

With DM = LOW (loudspeaker mode), inputs IS1 and IS2 determine the pulse duration of the output signal and thereby the DC resistance R_{xy} (seen at points x and y in Fig.8), the input impedance Z_i and also the Sound Pressure Level (SPL). The selection of 3 impedance settings and automatic swell is shown in Table 4.

Table 4 Setting of pulse duration and automatic swell (DM = LOW)

INPUT STATE		FUNCTION	RINGING BURST NUMBER (N)	PULSE DURATION(1) (μs)		R_{xy}(3) (kΩ)	Z_i(3) (kΩ)	SPL(2)(3) (dBr)
IS1	**IS2**			**t_{fund}**	**t_{harm}**			
LOW	LOW	automatic swell	1	1.9	–	40	tbf	tbf
			2	2.9	–	20	17.5	–4
			>2	4.1	1.8	5	7	0
LOW	HIGH	constant level	–	2.9	–	20	17.5	–4
HIGH	LOW		–	3.8	–	10	10.5	tbf
HIGH	HIGH		–	5.4	–	5	7	0

Notes

1. Typical pulse durations, t_{fund} and t_{harm}, for the delta-modulated approximation of fundamental and harmonic signals; valid for f_{OSC} = 64 kHz and f_{clk} = 32 kHz. See Fig.6 and Fig.7.
2. SPL is the relative Sound Pressure Level, and 0 dBr is defined as the SPL for IS1 = IS2 = HIGH.
3. Values of the DC resistance R_{xy}, bell impedance (Z_i) and SPL are valid for a value of input voltage $V_{i(rms)}$ = 40 V.

When IS1 and IS2 are both LOW, the circuit operates in the automatic swell mode. The SPL then increases in three steps so that the maximum level is reached for the third ringing burst.

Each time V_{DD} drops below V_{AS} the automatic swell register is reset and the next ringing burst is considered as N = 1 (see Table 4). A buffer capacitor (see Fig.8) must hold $V_{DD} > V_{AS}$ during the time between two consecutive ringing bursts of a series.

For each of the other three combinations of pins IS1 and IS2 the pulse duration has a constant value. Thus the ringer can be designed so that the impedance represented at the telephone line will comply with postal requirements that vary in relation to parallel or series connections of more than one ringer.

To satisfy some applications, a harmonic signal is added to the fundamental frequency in the last step of the automatic swell mode. The pulses representing this harmonic signal are interleaved with the pulses of the fundamental signal (see Fig.7). The difference in pulse duration shown in Table 4, is chosen so that the harmonic level is 10 dB below the fundamental level.

The harmonic frequency range is from 2 kHz to 3.2 kHz. The individual harmonic frequencies for the seven tone codes and the relative fundamental frequencies are shown in Table 5.

Table 5 Harmonic frequency in relation to tone code and fundamental frequency

TONE CODE	FREQUENCY (Hz)	
	FUNDAMENTAL	HARMONIC
1	533	3200
2	600	2400
3	667	2667
4	800	3200
5	1000	2000
6	1067	2133
7	1333	2667

Using a single mask it is possible to program the following:

- Addition of harmonics in all the other input states of IS1 and IS2
- All pulse duration values
- Other even harmonic frequencies.

7.10 Optical output (OPT)

The $\overline{\text{OPT}}$ output is designed to drive an optical signal transducer or lamp. It is LOW when the ringer circuit is enabled and HIGH when the ringer circuit is disabled. This output can also be used to switch the transmitter ON and OFF in the base unit of a cordless telephone set.

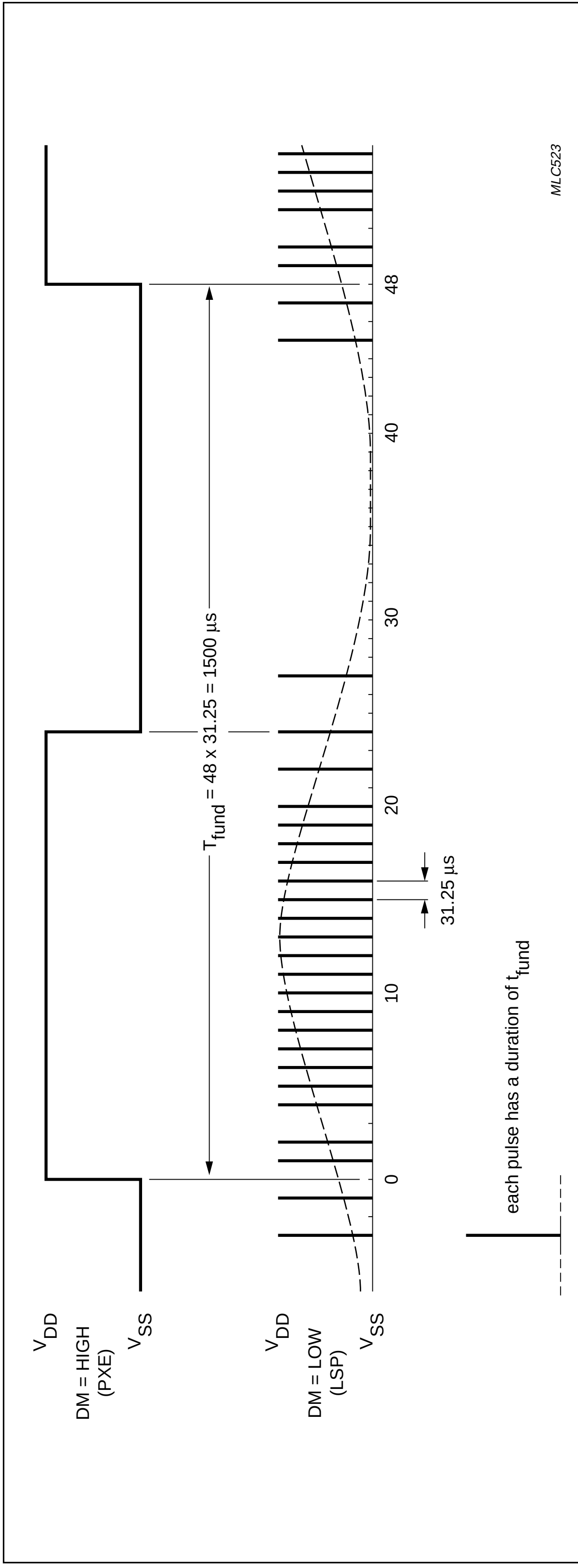


Fig.6 Fundamental signal (667 Hz) at pin TONE (for f_{OSC} = 64 kHz, to provide f_{clk} = 32 kHz). Square wave and delta-modulated options.

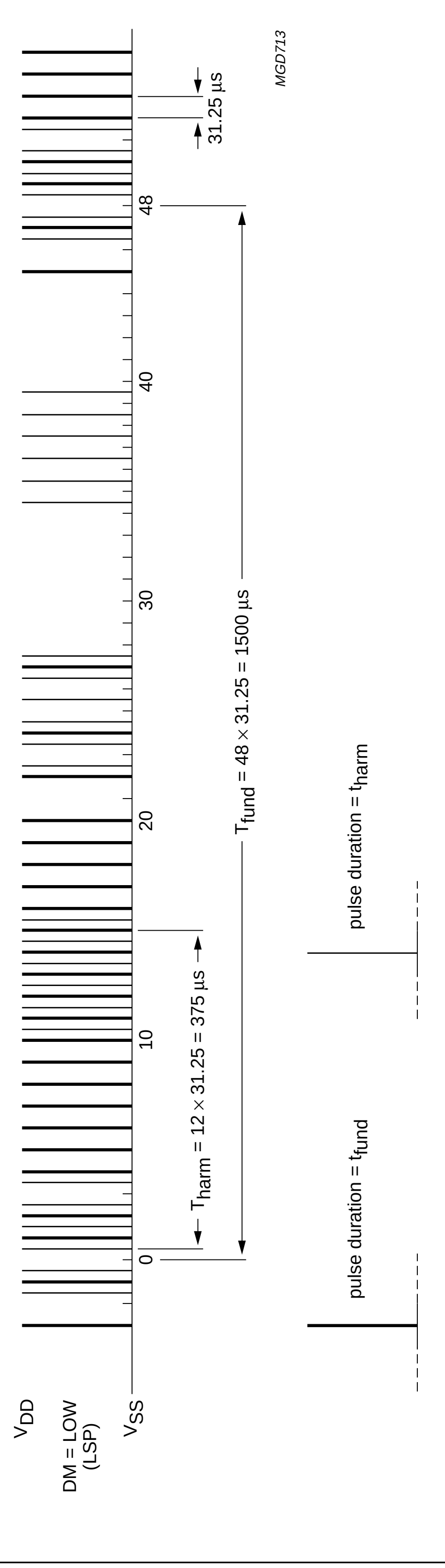


Fig.7 Fundamental signal (667 Hz) + harmonic signal (2667 Hz) at pin TONE (for f_{OSC} = 64 kHz, to provide f_{clk} = 32 kHz). Delta-modulated option.

8 LIMITING VALUES

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
V_{DD}	supply voltage	–0.8	+9	V
I_{DD}	supply current	–	50	mA
V_I	all input voltages	–0.8	V_{DD} + 0.8	V
I_I	DC input current	–10	+10	mA
I_O	DC output current	–10	+10	mA
P_{tot}	total power dissipation	–	300	mW
P_O	power dissipation per output	–	50	mW
T_{stg}	storage temperature range	–65	+150	°C
T_j	operating junction temperature	–25	+70	°C

9 HANDLING

Inputs and outputs are protected against electrostatic discharge in normal handling. However, it is good practice to take normal precautions appropriate to handling MOS devices. See *“Data Handbook IC03, General, Handling MOS devices”*.

10 DC CHARACTERISTICS

V_{DD} = 6.0 V; V_{SS} = 0 V; f_{OSC} = 64 kHz; T_{amb} = –25 to +70 °C; valid enable conditions at FDI and $\overline{FDE}$; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Supply						
V_{DD}	operating supply voltage		V_{stb} + 0.1	–	8.0	V
V_{stb}	standby supply voltage	note 1	3.9	4.8	5.7	V
V_{AS}	supply voltage for automatic swell reset	note 2		$0.5V_{stb}$		V
I_{DD}	operating supply current	note 3	–	110	140	µA
I_{stb}	standby supply current	$V_{DD} < V_{stb}$; note 4	–	3	8	µA
Inputs						
V_{IL}	LOW level input voltage		0	–	$0.3V_{DD}$	V
V_{IH}	HIGH level input voltage		$0.7V_{DD}$	–	V_{DD}	V
PULL-DOWN CIRCUIT OF INPUTS FDE, R1, RR2, DM, IS1, IS2, TS1, FL, FH						
R_{IL}	pull-down resistance	input at V_{SS}	–	20	–	kΩ
I_{IH}	pull-down current	input at V_{DD}	–	0.1	–	µA
PULL-DOWN CIRCUIT OF FDI						
I_{SL}	pull-down current (LOW)	$V_{FDI} = 0.3V_{DD}$; T_{amb} = 25 °C	14	23	32	µA
$TC_{(FDI)}$	temperature coefficient of I_{SL}	$V_{FDI} = 0.3V_{DD}$; T_{amb} = 25 °C	–	0.5	–	%/°C
I_{SH}	pull-down current (HIGH)	$V_{FDI} = 0.8V_{DD}$	–	0.1	–	µA
I_{SX}	pull-down current (STANDBY)	$V_{DD} < V_{stb}$	–	0.1	–	µA
I_{IS}	current into input FDI	note 5	–0.2	–	+0.2	mA
Outputs, TONE and $\overline{\text{OPT}}$						
I_{OL}	output sink current	V_{OL} = 0.5 V	1	2	–	mA
I_{OH}	output source current	V_{OL} = –0.5 V	–1	–2	–	mA

Notes

1. For $V_{DD} < V_{stb}$ the circuit is in standby mode.
2. At $V_{DD} = V_{AS}$ the automatic swell register is reset.
3. R_{OSC} = 365 kΩ; C_{OSC} = 56 pF; FDI = $\overline{FDE}$ = V_{DD}; all other inputs and outputs open-circuit; see Figs 8 and 9.
4. The standby supply current is measured with all inputs and outputs open-circuit, with the exception of OSC.
5. The current I_{IS} is clamped to V_{DD} and to V_{SS} by two internal diodes. Correct operation is ensured with $V_{FDI} > V_{DD}$ or $V_{FDI} < V_{SS}$, provided the maximum value of I_{IS} is not exceeded. (The input FDI has an extended HIGH and LOW input voltage range.)

11 AC CHARACTERISTICS

V_{DD} = 6.0 V; V_{SS} = 0 V; f_{OSC} = 64 kHz; T_{amb} = –25 to +70 °C; valid enable conditions at FDI and $\overline{FDE}$; all voltages with respect to V_{SS}; unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$t_{d(on)}$	switch-on delay	$\overline{FDE}$ = LOW; ringing frequency within limit set by FL and FH; note 1	1	–	1.5	cycle
$t_{d(off)}$	switch-off delay	FL = LOW	–	–	50	ms
		FL = HIGH	–	–	75	ms
f_{OSC}	oscillator frequency	R_{OSC} = 365 kW; C_{OSC} = 56 pF; T_{amb} = 25 °C; note 2	60	64	68	kHz
$\Delta f_{OSC}/\Delta V_P$	oscillator frequency variation with respect to supply voltage		–	1	–	%/V
$\Delta f_{OSC}/\Delta T$	oscillator frequency variation with respect to temperature		–	0.05	–	%/K

Notes

1. The switch-on delay is measured in cycles of incoming ringing frequency.
2. Lead lengths of R_{OSC} and C_{OSC} to be kept to a minimum.

12 APPLICATION INFORMATION

Application of the PCD3360 in a telephone ringer circuit together with a loudspeaker is shown in Fig.8.
The threshold levels V_H and V_L of the frequency discriminator circuit are determined by:

- The logic threshold of input FDI (0.5V_{DD}, typically 3.4 V for V_{DD} = 6.8 V)
- The pull-down current of input FDI (20 µA typically for FDI < 3.4 V)
- The value of R2 (680 kΩ in Fig.8).

For a positive slope the voltage at R2 must exceed the value V_H before FDI will become HIGH; V_H is the sum of the input threshold and the voltage drop across R2 thus:

$$V_H = 3.4 + \left(680 \times 10^{-3}\right) \times \left(20 \times 10^{-6}\right) = 17\ \text{V}$$

For a negative slope, the voltage at R2 must decrease below the value of V_L before FDI will become LOW. Because the current into FDI is negligible with FDI = HIGH the voltage drop across R2 can be discounted, thus V_L = 3.4 V.

The minimum operating voltage across C3 is 17.8 V which is determined by:

- The minimum operating voltage of the PCD3360 (5.8 V)
- The supply current of the PCD3360 (120 µA max.)
- The value of R3 (100 kΩ in Fig.8).

The total switch-on delay equals approximately the time required to charge the supply capacitor C3 to the minimum operating value, plus the specified switch-on delay of the PCD3360.

The high operating voltage combined with the class D output stage ensures the optimal energy conversion and thereby a high sound level. The design can easily be optimized for parallel or series connection of more than one ringer. The diode bridge, zener diode (D1) and resistor R1 protect the ringer against transients up to 5 kV. During these surges the voltage on the 68 V zener diode (BZW03-C68) can rise to 100 V; the DMOS transistor BST72A (TR1) has a maximum drain-source voltage of 100 V. Up to 220 V, 50 Hz can be applied to the a/b terminals without damaging the ringer.

The choke (L1) in series with the 50 Ω loudspeaker increases the sound pressure level by approximately 3 dB by suppression of the 32 kHz carrier frequency and its sidebands. The flyback diode BAX18A (D2) is a fast type with low forward voltage to obtain high efficiency.

Application of the PCD3360 together with a PXE transducer is shown in Fig.9. The only significant difference between Fig.8 and Fig.9 is the output stage. Two BST72A transistors provide an output voltage swing almost equal to the voltage at C3. Pins IS1 and IS2 are inoperative because DM = HIGH. Volume control is possible using resistor R_V.

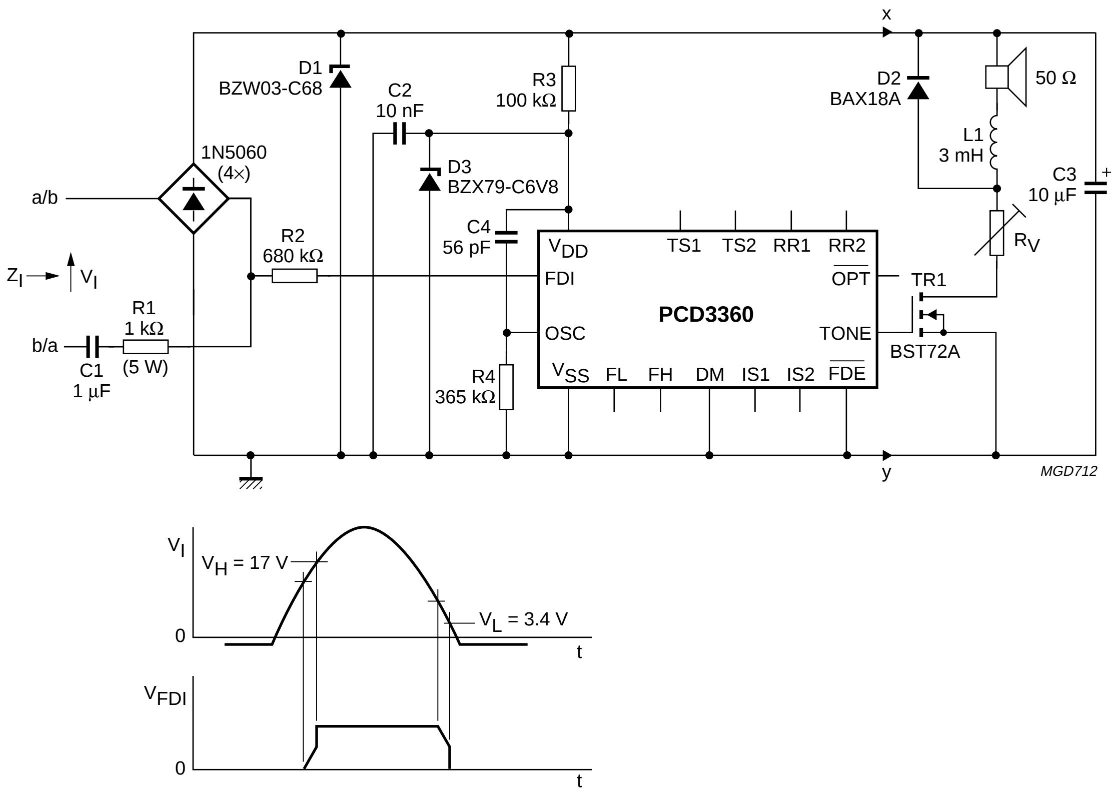


Fig.8 Transformerless electronic ringer with PCD3360 and a loudspeaker.

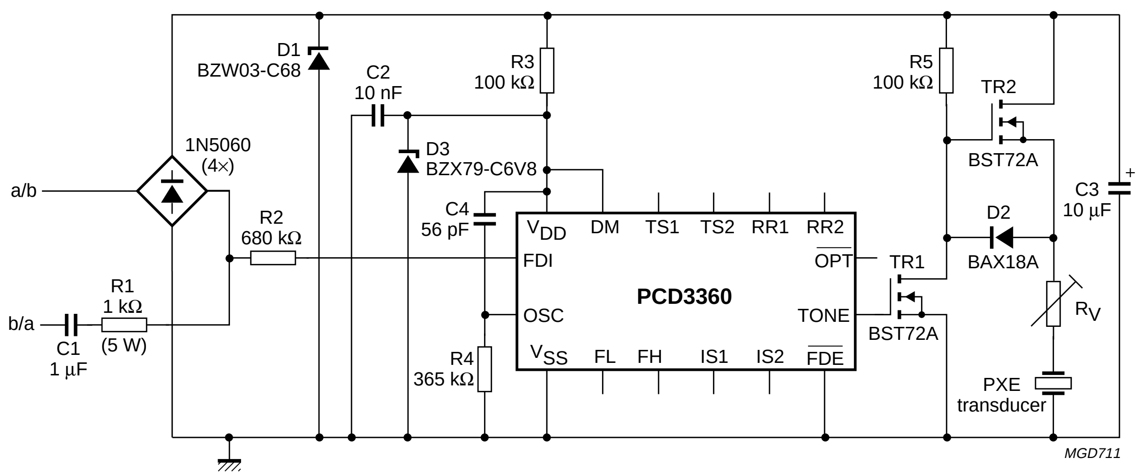
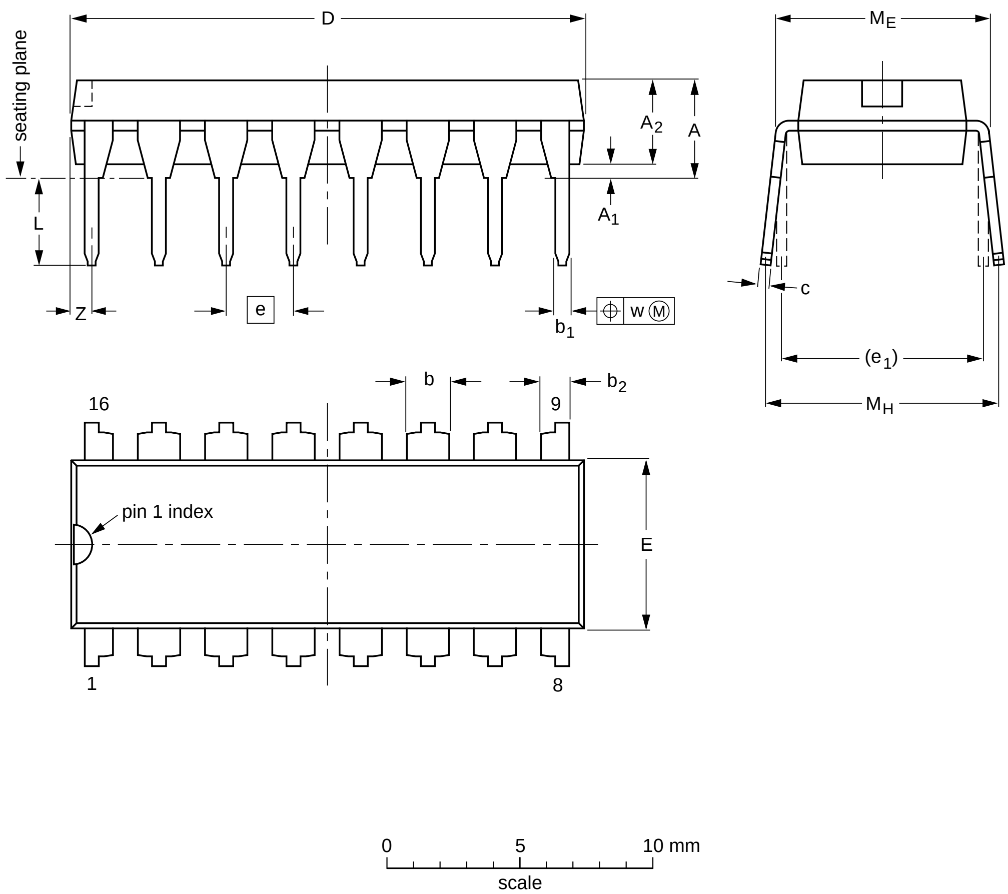


Fig.9 PCD3360 ringer with PXE transducer.

13 PACKAGE OUTLINES

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

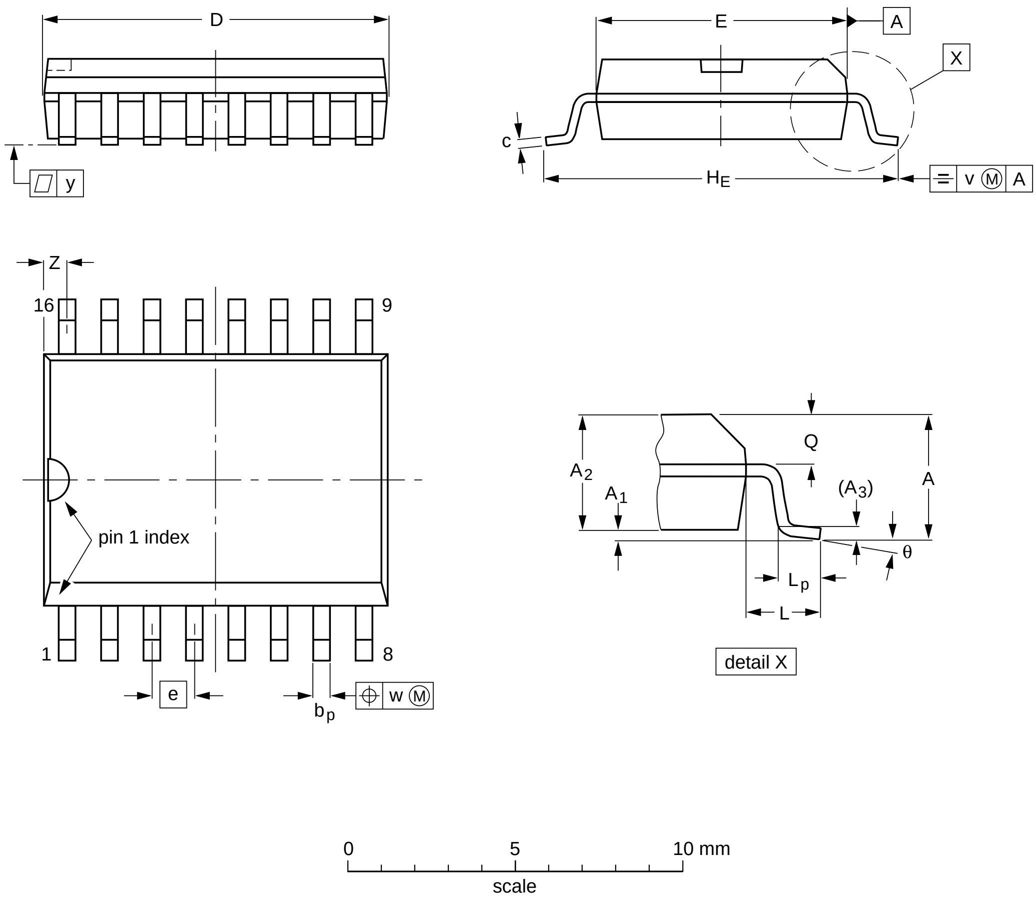
UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.030

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT38-4						~~92-11-17~~ 95-01-14

SO16: plastic small outline package; 16 leads; body width 7.5 mm **SOT162-1**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D (1)	E (1)	e	H_E	L	L_p	Q	v	w	y	Z (1)	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	10.5 10.1	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8^o 0^o
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.41 0.40	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT162-1	075E03	MS-013AA				~~92-11-17~~ 95-01-24

14 SOLDERING

14.1 Introduction

There is no soldering method that is ideal for all IC packages. Wave soldering is often preferred when through-hole and surface mounted components are mixed on one printed-circuit board. However, wave soldering is not always suitable for surface mounted ICs, or for printed-circuits with high population densities. In these situations reflow soldering is often used.

This text gives a very brief insight to a complex technology. A more in-depth account of soldering ICs can be found in our *"IC Package Databook"* (order code 9398 652 90011).

14.2 DIP

14.2.1 SOLDERING BY DIPPING OR BY WAVE

The maximum permissible temperature of the solder is 260 °C; solder at this temperature must not be in contact with the joint for more than 5 seconds. The total contact time of successive solder waves must not exceed 5 seconds.

The device may be mounted up to the seating plane, but the temperature of the plastic body must not exceed the specified maximum storage temperature ($T_{stg\ max}$). If the printed-circuit board has been pre-heated, forced cooling may be necessary immediately after soldering to keep the temperature within the permissible limit.

14.2.2 REPAIRING SOLDERED JOINTS

Apply a low voltage soldering iron (less than 24 V) to the lead(s) of the package, below the seating plane or not more than 2 mm above it. If the temperature of the soldering iron bit is less than 300 °C it may remain in contact for up to 10 seconds. If the bit temperature is between 300 and 400 °C, contact may be up to 5 seconds.

14.3 SO

14.3.1 REFLOW SOLDERING

Reflow soldering techniques are suitable for all SO packages.

Reflow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed-circuit board by screen printing, stencilling or pressure-syringe dispensing before package placement.

Several techniques exist for reflowing; for example, thermal conduction by heated belt. Dwell times vary between 50 and 300 seconds depending on heating method. Typical reflow temperatures range from 215 to 250 °C.

Preheating is necessary to dry the paste and evaporate the binding agent. Preheating duration: 45 minutes at 45 °C.

14.3.2 WAVE SOLDERING

Wave soldering techniques can be used for all SO packages if the following conditions are observed:

- A double-wave (a turbulent wave with high upward pressure followed by a smooth laminar wave) soldering technique should be used.
- The longitudinal axis of the package footprint must be parallel to the solder flow.
- The package footprint must incorporate solder thieves at the downstream end.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured.

Maximum permissible solder temperature is 260 °C, and maximum duration of package immersion in solder is 10 seconds, if cooled to less than 150 °C within 6 seconds. Typical dwell time is 4 seconds at 250 °C.

A mildly-activated flux will eliminate the need for removal of corrosive residues in most applications.

14.3.3 REPAIRING SOLDERED JOINTS

Fix the component by first soldering two diagonally-opposite end leads. Use only a low voltage soldering iron (less than 24 V) applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300 °C. When using a dedicated tool, all other leads can be soldered in one operation within 2 to 5 seconds between 270 and 320 °C.

15 DEFINITIONS

Data sheet status	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
Limiting values	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
Application information	
Where application information is given, it is advisory and does not form part of the specification.	

16 LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips for any damages resulting from such improper use or sale.

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Philips Semiconductors – a worldwide company

Argentina: see South America

Australia: 34 Waterloo Road, NORTH RYDE, NSW 2113,
Tel. +61 2 9805 4455, Fax. +61 2 9805 4466

Austria: Computerstr. 6, A-1101 WIEN, P.O. Box 213,
Tel. +43 1 60 101, Fax. +43 1 60 101 1210

Belarus: Hotel Minsk Business Center, Bld. 3, r. 1211, Volodarski Str. 6,
220050 MINSK, Tel. +375 172 200 733, Fax. +375 172 200 773

Belgium: see The Netherlands

Brazil: see South America

Bulgaria: Philips Bulgaria Ltd., Energoproject, 15th floor,
51 James Bourchier Blvd., 1407 SOFIA,
Tel. +359 2 689 211, Fax. +359 2 689 102

Canada: PHILIPS SEMICONDUCTORS/COMPONENTS,
Tel. +1 800 234 7381

China/Hong Kong: 501 Hong Kong Industrial Technology Centre,
72 Tat Chee Avenue, Kowloon Tong, HONG KONG,
Tel. +852 2319 7888, Fax. +852 2319 7700

Colombia: see South America

Czech Republic: see Austria

Denmark: Prags Boulevard 80, PB 1919, DK-2300 COPENHAGEN S,
Tel. +45 32 88 2636, Fax. +45 31 57 1949

Finland: Sinikalliontie 3, FIN-02630 ESPOO,
Tel. +358 9 615800, Fax. +358 9 61580/xxx

France: 4 Rue du Port-aux-Vins, BP317, 92156 SURESNES Cedex,
Tel. +33 1 40 99 6161, Fax. +33 1 40 99 6427

Germany: Hammerbrookstraße 69, D-20097 HAMBURG,
Tel. +49 40 23 53 60, Fax. +49 40 23 536 300

Greece: No. 15, 25th March Street, GR 17778 TAVROS/ATHENS,
Tel. +30 1 4894 339/239, Fax. +30 1 4814 240

Hungary: see Austria

India: Philips INDIA Ltd, Shivsagar Estate, A Block, Dr. Annie Besant Rd.
Worli, MUMBAI 400 018, Tel. +91 22 4938 541, Fax. +91 22 4938 722

Indonesia: see Singapore

Ireland: Newstead, Clonskeagh, DUBLIN 14,
Tel. +353 1 7640 000, Fax. +353 1 7640 200

Israel: RAPAC Electronics, 7 Kehilat Saloniki St, TEL AVIV 61180,
Tel. +972 3 645 0444, Fax. +972 3 649 1007

Italy: PHILIPS SEMICONDUCTORS, Piazza IV Novembre 3,
20124 MILANO, Tel. +39 2 6752 2531, Fax. +39 2 6752 2557

Japan: Philips Bldg 13-37, Kohnan 2-chome, Minato-ku, TOKYO 108,
Tel. +81 3 3740 5130, Fax. +81 3 3740 5077

Korea: Philips House, 260-199 Itaewon-dong, Yongsan-ku, SEOUL,
Tel. +82 2 709 1412, Fax. +82 2 709 1415

Malaysia: No. 76 Jalan Universiti, 46200 PETALING JAYA, SELANGOR,
Tel. +60 3 750 5214, Fax. +60 3 757 4880

Mexico: 5900 Gateway East, Suite 200, EL PASO, TEXAS 79905,
Tel. +9-5 800 234 7381

Middle East: see Italy

Netherlands: Postbus 90050, 5600 PB EINDHOVEN, Bldg. VB,
Tel. +31 40 27 82785, Fax. +31 40 27 88399

New Zealand: 2 Wagener Place, C.P.O. Box 1041, AUCKLAND,
Tel. +64 9 849 4160, Fax. +64 9 849 7811

Norway: Box 1, Manglerud 0612, OSLO,
Tel. +47 22 74 8000, Fax. +47 22 74 8341

Philippines: Philips Semiconductors Philippines Inc.,
106 Valero St. Salcedo Village, P.O. Box 2108 MCC, MAKATI,
Metro MANILA, Tel. +63 2 816 6380, Fax. +63 2 817 3474

Poland: Ul. Lukiska 10, PL 04-123 WARSZAWA,
Tel. +48 22 612 2831, Fax. +48 22 612 2327

Portugal: see Spain

Romania: see Italy

Russia: Philips Russia, Ul. Usatcheva 35A, 119048 MOSCOW,
Tel. +7 095 755 6918, Fax. +7 095 755 6919

Singapore: Lorong 1, Toa Payoh, SINGAPORE 1231,
Tel. +65 350 2538, Fax. +65 251 6500

Slovakia: see Austria

Slovenia: see Italy

South Africa: S.A. PHILIPS Pty Ltd., 195-215 Main Road Martindale,
2092 JOHANNESBURG, P.O. Box 7430 Johannesburg 2000,
Tel. +27 11 470 5911, Fax. +27 11 470 5494

South America: Rua do Rocio 220, 5th floor, Suite 51,
04552-903 São Paulo, SÃO PAULO - SP, Brazil,
Tel. +55 11 821 2333, Fax. +55 11 829 1849

Spain: Balmes 22, 08007 BARCELONA,
Tel. +34 3 301 6312, Fax. +34 3 301 4107

Sweden: Kottbygatan 7, Akalla, S-16485 STOCKHOLM,
Tel. +46 8 632 2000, Fax. +46 8 632 2745

Switzerland: Allmendstrasse 140, CH-8027 ZÜRICH,
Tel. +41 1 488 2686, Fax. +41 1 481 7730

Taiwan: Philips Semiconductors, 6F, No. 96, Chien Kuo N. Rd., Sec. 1,
TAIPEI, Taiwan Tel. +886 2 2134 2870, Fax. +886 2 2134 2874

Thailand: PHILIPS ELECTRONICS (THAILAND) Ltd.,
209/2 Sanpavuth-Bangna Road Prakanong, BANGKOK 10260,
Tel. +66 2 745 4090, Fax. +66 2 398 0793

Turkey: Talatpasa Cad. No. 5, 80640 GÜLTEPE/ISTANBUL,
Tel. +90 212 279 2770, Fax. +90 212 282 6707

Ukraine: PHILIPS UKRAINE, 4 Patrice Lumumba str., Building B, Floor 7,
252042 KIEV, Tel. +380 44 264 2776, Fax. +380 44 268 0461

United Kingdom: Philips Semiconductors Ltd., 276 Bath Road, Hayes,
MIDDLESEX UB3 5BX, Tel. +44 181 730 5000, Fax. +44 181 754 8421

United States: 811 East Arques Avenue, SUNNYVALE, CA 94088-3409,
Tel. +1 800 234 7381

Uruguay: see South America

Vietnam: see Singapore

Yugoslavia: PHILIPS, Trg N. Pasica 5/v, 11000 BEOGRAD,
Tel. +381 11 625 344, Fax.+381 11 635 777

For all other countries apply to: Philips Semiconductors, Marketing & Sales Communications,
Building BE-p, P.O. Box 218, 5600 MD EINDHOVEN, The Netherlands, Fax. +31 40 27 24825

Internet: http://www.semiconductors.philips.com

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